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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,325	07/07/2003	Dean A. Klein	MTIPAT.074C1D1	9352
20995	7590	12/02/2004	EXAMINER	
KNOBBE MARTENS OLSON & BEAR LLP 2040 MAIN STREET FOURTEENTH FLOOR IRVINE, CA 92614			NGUYEN, HIEP T	
			ART UNIT	PAPER NUMBER
			2187	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/615,325

Applicant(s)

KLEIN, DEAN A.

Examiner

Hiep T Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 9/15/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Connolly et al, U.S.

Patent No. 5,802,395 [hereafter, Connolly].

- a. As per claim 1: Connolly teaches a method of accessing data storage locations in a memory circuit comprising the acts of:
 - i. issuing at least one memory access control signal to a first portion of said memory circuit [i.e., the issuing of the RAS and/or CAS to the ASIC 310 of the memory circuit; figure 3; col. 3, lines 4-6]; and
 - ii. coupling a data bus to a second portion of said memory circuit in response to said at least one memory access control signal [col. 3, lines 50-63].
- b. As per claim 2: Connolly further teaches the further claimed limitation of "wherein issuing at least one memory access control signal comprises issuing a row address strobe signal and a column address strobe signal" [see again col. 3, lines 4-6 and 50-63].
- c. As per claim 3: Connolly al teach the further claimed limitation of "wherein issuing at least one memory access control signal comprises issuing a memory circuit enable signal".

This is because it has been known in the pertinent art that CAS and CAS are signals

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provided to a semiconductor memory such as that of Connolly to function as enabling signals for introducing row and column address information into the memory [see U.S. patent 4,792,929, col. 1, lines 36-40, for example].

- d. As per claim 4: Connolly further teaches the claimed limitation of "wherein coupling a data bus comprises closing a transfer gate in each line of said data bus" [see figure 2; col. 3, lines 45-49].
- e. As pre claim 5: similarly to claims 1-4, Connolly teaches a method of accessing data storage locations in a memory circuit comprising the acts of [see again col. 3, lines 4-6 and 50-63; figures 2-3]:
 - i. issuing at least one memory access control signal to a first portion of said memory circuit, the signal comprising a row address strobe signal and a column address strobe signal; and
 - ii. coupling a data bus to a second portion of said memory circuit in response to said at least one memory access control signal, the coupling comprising closing a transfer gate in each line of said data bus.
- f. As per claim 6: similarly to claim 1, Connolly teaches a system [figure 1] for accessing data storage locations in a memory circuit [20-40] comprising the acts of [see again col. 3, lines 4-6 and 50-63; and figures 1-3]:
 - i. means (109) for issuing at least one memory access control signal to a first portion of said memory circuit; and
 - ii. means (309, 319, 409, 419) for coupling a data bus to a second portion of said memory circuit in response to said at least one memory access control signal.
- g. As per claim 7: similarly to claim 2, Connolly further teaches the claimed limitation of "wherein the means for issuing at least one memory access control signal comprises means for issuing a row address strobe signal and a column address strobe signal [see again, figure 3, col. 3, lines 4-6 and 50-63].

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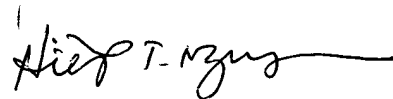
- h. As per claim 8: similarly to claim 3, Connolly also teaches the further claimed limitation of “wherein the means for issuing at least one memory access control signal comprises means for issuing a memory circuit enable signal [see again the comment in the rejection of claim 3, above].
- i. As per claim 9: similarly to claim 4, Connolly further teaches that claimed limitation of “wherein the means for coupling a data bus comprises means for closing a transfer gate in each line of said data bus [see again figure 2, and the comment in the rejection of claim 4].
- j. As per claims 10-15, similarly to claims 1-9, above, each and every claimed elements and limitations has already been addressed above. Accordingly, Connolly also teaches the claimed system or device in claims 10-15.

Conclusion

- 4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
 - a. Olson et al., U.S. Patent No. 4,792,929, teaches that CAS and CAS are signals provided to a semiconductor memory such as that of Connolly to function as enabling signals for introducing row and column address information into the memory.
- 5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep T Nguyen whose telephone number is (571) 272-4197. The examiner can normally be reached on Monday-Friday from 9:30 am to 6:00 pm.
- 6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Hiep T Nguyen
Primary Examiner
Art Unit 2187

HTN